Thank you for taking the Week 11 : Assignment 11.

Week 11 : Assignment 11

Your last recorded submission was on 2021-10-11, 13:54 IST

Due date: 2021-10-13, 23:59 IST.

1) Consider a 5-stage instruction pipeline with stage delays of 20 nsec, 25 nsec, 35 nsec, 30 nsec, and 22 nsec respectively. The delay of an inter-stage register stage of the pipeline is 2 nsec. The total time required for the execution of 1000 instructions will be ..... microseconds.

37.15

1 point

2) Consider a 3-stage instruction pipeline with stage delays of 25 nsec, 30 nsec and 15 nsec respectively, and the delay of an inter-stage register stage of 5 nsec. Suppose the pipeline is modified by splitting the 1st stage into two simpler stages with delays 10 nsec and 15 nsec, and 2nd stage into two simpler stages with delays 15 nsec and 15 nsec. For the execution of 1000 instructions, the speedup of the new 5-stage pipeline over the previous 3-stage pipeline will be _____.

1.75

1 point

3) Consider a non-pipelined CPU working at 1GHz clock. The frequency of ALU operations, branches and memory operations are 50%, 25% and 25% respectively. If ALU and memory operations take 4 cycles and branch operation takes 7 cycles, the average instruction execution time will be ..... nsec.

4.75

1 point

4) Which of the following statement(s) is/ are true? *1 point*

a. Pipeline hazards prevent pipeline from operating at its maximum possible speed.
b. Data hazard arise due to resource conflicts.
c. Control hazard arise due to branch and other instructions that change the PC.
d. All of these.

- [x] a.
- [ ] b.
- [x] c.
- [ ] d.

5) Consider a non-pipelined processor with a clock rate of 4 GHz and average cycles per instruction of 10. The same processor is upgraded to a 6-stage pipelined processor but due to the internal pipeline delay, the clock rate is reduced to 2 GHz. Assume there are no stalls in the pipeline. The speed up achieved in this pipelined processor will be .....

5 *1 point*

6) Consider the execution of following instructions in a 5-stage MIPS pipeline (IF, ID, EX, MEM, WB): *1 point*

1: ADD R2, R5, R8

2: MUL R1, R4, R5

3: SUB R9, R2, R6

4: ADD R1, R5, R6

The **Read After Write** (RAW) data dependency exist between which pair of instructions that can lead to data hazard?

a. 1 and 2
b. 1 and 3
c. 2 and 3
d. 2 and 4

- ( ) a.
- (•) b.
- ( ) c.
- ( ) d.

7) For the following MIPS32 program segment, how many stall cycles will be required .....?

1: LW R5, 200(R2)

2: ADD R1, R6, R8

3: SUB R3, R5, R8

2

1 point

8) Which of the following data hazards can cause performance degradation in the MIPS32 integer pipeline?

1 point

a. WAR data hazard.
b. WAW data hazard.
c. RAW data hazard.
d. Memory load followed by use of the loaded data.

- [ ] a.
- [ ] b.
- [x] c.
- [x] d.

9) Consider the MIPS32 pipeline with ideal CPI of 1.5. Assume that 30% of all instructions executed are branch, out of which 90% are taken branches. The pipeline speedup for (i) predict taken and (ii) predict not taken approaches to reduce branch penalties will be approximately:

1 point

a. 3.94, 3.85
b. 4.34, 4.29
c. 3.85, 4.34
d. 3.85, 3.94

- ○ a.
- ○ b.
- ○ c.
- ◉ d.

10) In a MIPS pipeline with Branch Target Buffer (BTB), assume that 85% of the branches are found in BTB, 15% of the predictions are incorrect, and 75% of the branches are taken. The branch penalty will be ..... clock cycles.

0.52

1 point

You may submit any number of times before the due date. The final submission will be considered for grading.

Submit Answers

Note: All these answers are confirmed from our side, we don't guarantee that you will get a 100% score. These are our own answers that we are sharing with you all. If you have any doubt that our answers are not correct then feel free to discuss (in-group) or do your own answer.

Most important: We don't promote any type of cheating, these answers are only for those students who are not able to do it on their own or need some help.